REMARKS

Claims 1-7 are presented for examination. No amendments have been made to the claims.

The applicants respectfully submit that no new matter has been added. It is believed that this Amendment is fully responsive to the Office Action dated **May 19, 2006**.

The applicants thank the Examiner for the helpful guidance provided during a telephone discussion held on August 16, 2006. In accordance with that discussion, an English translation of the relevant portions of **JP 59-78654** is attached to this amendment.

The present invention recited in claims 1-7 define a chip mount area (42) of a flexible lead (41) extending from a main display (4), and a chip mount area (53) of a flexible lead (51) extending from a subdisplay (5), the chip mount areas being opposed to each other in an opening of a frame (6). In order to solve the inherently difficult problem of arranging electronic parts facing an opening of a frame that holds two LCD panels, claims 1-7 define a foldable electronic device wherein a reduction in thickness of the device is realized through opposite arrangement of chip mount areas in a frame. In particular, the chip mount areas are oppositely positioned in an opening of a frame that holds a main display and a subdisplay so that groups of electronic chips mounted on the chip mount areas are also oppositely positioned and, additionally, in a meshed and staggered relationship. Due to the meshed and staggered arrangement of the electronic chips, the two chip mount areas can be

oppositely arranged and can fit in an opening of the frame which also holds the main display and subdisplay.

Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kweon, et al. in view of the cited prior art document JP 59-78654.

Kweon discloses a folder-type mobile communication terminal having double-sided LCD. The Office Action asserts that **Kweon** teaches a frame provided inside a closure which secures a main display and a subdisplay as arranged "back to back" with chip mount areas being opposed to each other in an opening formed in a frame with the opposed surfaces of the respective chip mount areas having groups of electronic chips mounted thereon, and cites as support Fig. 3 (24) (frame), Fig. 5 (21, 22, 24) (frame inside a closure), Fig. 1-3 (main and subdisplay arrangement), and Fig. 3 (27,28), Fig. 5 (opposed surfaces of chip mount areas). The Office Action concedes that **Kweon** fails to disclose groups of electronic circuit chips positioned in a staggered relation to each other, and cites **JP 59-78654** for the disclosure. **JP 59-78654** teaches a printed circuit board wherein a printed wiring board is curved concavely and convexly, having circuit components mounted on both concave and convex areas of the printed wiring board. In particular, the Office Action refers to Fig. 3 as describing a staggered relationship between groups of electronic circuit chips.

Kweon and **JP 59-78654** fail to teach the present invention recited in claims 1-7 because no motivation exists to combine the references given that by design **Kweon** specifically teaches LCD panels separated by a light guide plate**.** Contrary to the Office Action's assertion, **Kweon** fails to

teach or suggest chip mount areas positioned *directly next to each other* in an opening of a frame. According to Figs. 3 and 5 of **Kweon**, the chip mount areas (27, 28) are clearly separated by a light guide plate 23: "Two LCD panels 27 and 28 of inside and outside of the flip are symmetrically equipped with the *backlight in the center*." (Kweon, col.3, lines 15-17). The light guide plate 23, which provides light to the LCD panels (27, 28) are necessary to the operation of the invention of **Kweon**. (Kweon, col.2, lines 12-17, col. 3, lines 17-25). In other words, in **Kweon**, the chip mount areas (27, 28) are *necessarily separated*, and not positioned *directly next to each other* in an opening of a frame, as in the present invention. Given that **Kweon**'s disclosure centers around two LCD panels separated by a shared backlight, no motivation exists to combine this reference with **JP 59-78654** which would require the chip mount areas to be oppositely positioned with no separation in order to achieve a meshed and staggered arrangement of oppositely facing electronic chips.

Furthermore, **JP 59-78654** fails to disclose any opposed relationship of parts in an opening of a frame. In the claimed invention, however, a reduction in thickness of a device is achieved by oppositely arranging components in an opening of a frame.

Kweon and **JP 59-78654** fail to teach the present invention recited in claims 1-7 because in combination, the references fail to teach chip mount areas oppositely positioned *directly next to each other* so that the opposite positioning results in a meshed and staggered relationship between groups of electronic chips mounted thereon, thereby achieving a reduction in thickness of the chip mount areas located in the frame.

The previous Office Action cited **Antila** (U.S. Patent No. 6,583,770) for the disclosure of a

frame holding a main display and subdisplay oriented mounted back to back, and pointed to Fig. 3 (17, D1, D2) and col.5, lines 62-63 as support. However, as the applicants discussed in the amendment filed on February 8, 2006, **Antila** discloses an electronic folding device having a two-sided display in which the thickness of the display construction is reduced by using *a component common to both sides* of the display. That is, Fig. 3 of **Antila** does not teach two displays located in a frame. As for Fig. 2 of **Antila**, the device described therein discloses chip mount areas (Dr', Dr") positioned back to back, not back-to-back arrangement of a main display and a subdisplay. In the claimed invention, however, the main display (4) and the subdisplay (5) are arranged back to back, rather than the two chip mount areas (42, 53). In addition, **Antila** fails to disclose chip mount areas positioned in an opening formed in a frame that holds a main display and a subdisplay. Therefore, **Antila** fails to teach or suggest the claimed invention as well.

For the reasons discussed above, it is respectfully requested that this rejection be reconsidered and withdrawn.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact the applicants undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, the applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other

fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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(Partial translation)
Japanese Unexamined Laid-open Utility Model Publication No. S59-78654

(Page 1, line 17- page 3, line 9)
3. Detail description of the invention

This invention relates to a component mounting board for electronics devices, etc., capable of enhancing the spatial packaging density in mounting electronics circuit components in high density.

As a conventional component mounting board, as shown in Fig. 1, a board in which discrete components such as chips, e.g., ICs, or Hybrid ICs (hereinafter referred to as "HIC") and chemical capacitors are mounted on a hard resin board made of, e.g., paper-phenol, glass, or epoxy resin has been used. In Fig. 1, (1) denotes a resin board made of, e.g., paper-phenol, glass, or epoxy resin, and (2) to (6) denote circuit components such as chemical capacitors, ICs, coils, HICs, or chip components mounted on the board (1).

As shown in Fig. 1, the circuit components (2)(3)(4)(5)(6) mounted on the resin board (1) are different in shape and size, and therefore the spatial packaging density cannot be increased so much. Furthermore, in the case of using a plurality of component mounting boards, as shown in Fig. 2, a method in which adjacent boards are combined with the concave-convex portions of components on the adjacent boards arranged reversely to improve the spatial packaging density has been employed. In this case, however, since the component placement cannot be determined until the concave-convex portions of the adjacent boards are specified, there are such drawbacks that the boards to be combined should be designed simultaneously and that it becomes difficult to utilize the space using the concave-convex portions if the component positional change is difficult due to the circuit structure, resulting in a failure of highly increased spatial packaging density.

This invention was made to overcome the aforementioned conventional drawbacks, and aims to provide a component mounting board enhanced in spatial packaging density by bending a circuit board for mounting circuit components in a concave-convex manner and mounting circuit components on the circuit board such that heights of circuit components mounted on concave portions of the circuit board are higher than heights of circuit components mounted on convex portions.

(Page 5, lines 12-16)
4. Brief description of drawings

Fig. 1 is a side view showing an example of a conventional component mounting board. Fig. 2 is a side view showing a structure for increasing the spatial packaging density using a plurality of conventional component mounting boards shown in Fig. 1.